Amendments to the Claims:

1. (Currently Amended) A method of performing built-in self repair of memories comprising:

loading a value into an on-chip counter through a test pattern during production testing, where the value represents an amount of redundant elements which are allowed for a repair;

testing the memories a first time;

generating a repair solution;

identifying memories which require a number of redundant elements for repair which exceeds the value that has been loaded into the on-chip counter;

using the repair solution to repair a first set of damaged memories while not repairing and instead flagging a second set of damaged memories, wherein each of the memories in the second set have been ~~determined to require~~ identified as requiring a number of redundant elements to be used for the repair, where the number exceeds the value which has been loaded into the on-chip counter;

making an on-chip assessment to test the memories a second time; and

using the repair solution to repair damaged memories which were not previously flagged.

2. (Cancelled)

3. (Previously Presented) The method as recited in claim 1, further comprising loading the counter through a test pattern during production testing.

4. (Original) The method as recited in claim 1, further comprising loading a pre-determined repair solution into registers, testing the memories, and thereafter initiating the repair solution to repair the memories.

5. (Original) The method as recited in claim 4, further comprising using a reliability controller to test and repair the memories.

6. (Original) The method as recited in claim 5, said reliability controller comprising logic, at least one counter in communication with said logic, and a register set in communication with said logic.

7. (Original) The method as recited in claim 6, wherein said at least one counter comprises a first counter which contains the number of memories to be allowed for repair.

8. (Original) The method as recited in claim 7, further comprising loading a value into the register set which indicates the total number of memories.

9. (Original) The method as recited in claim 8, further comprising loading another value into the register set which indicates the maximum number of flare register bits among the memories.

10. (Original) The method as recited in claim 9, further comprising having the logic use the two values to create sections of patterns for each memory.

11. (Original) The method as recited in claim 10, wherein a start of each section contains redundant usage information.

12. (Currently Amended) A reliability controller configured for use in connection with built-in self repair of memories, said reliability controller configured to:

load a value into an on-chip counter through a test pattern during production testing, where the value represents an amount of redundant elements which are allowed for a repair;

test the memories a first time;

generate a repair solution;

identify memories which require a number of redundant elements for repair which exceeds the value that has been loaded into the on-chip counter;

use the repair solution to repair a first set of damaged memories while not repairing and instead flagging a second set of damaged memories, wherein each of the memories in the second set have been ~~determined to require~~ identified as requiring a number of redundant elements to be used for the repair, where the number exceeds the value which has been loaded into the on-chip counter;

make an on-chip assessment to test the memories a second time; and

use the repair solution to repair damaged memories which were not previously flagged.

13. (Original) The reliability controller as recited in claim 12, said reliability controller comprising logic, at least one counter in communication with said logic, and a register set in communication with said logic.

14. (Original) The reliability controller as recited in claim 13, wherein said at least one counter comprises a first counter which contains the number of memories to be allowed for repair.

15. (Original) The reliability controller as recited in claim 14, wherein the register set is configured to receive a value which indicates the total number of memories.

16. (Original) The reliability controller as recited in claim 15, wherein the register set is configured to receive a value which indicates the maximum number of flare register bits among the memories.

17. (Original) The reliability controller as recited in claim 16, wherein the logic is configured to use the two values to create sections of patterns for each memory.

18. (Original) The reliability controller as recited in claim 17, wherein a start of each section contains redundant usage information.